

REMARKS

Claims 67-92 are pending. Claims 67-92 stand rejected. Claim 67 has been amended.

Claims 68 and 70 stand rejected under 35 U.S.C. § 112, second paragraph lacking sufficient antecedent basis for the limitation "said act of positioning..." This rejection is respectfully traversed.

Claim 68 has been amended to recite, *inter alia*, a "method comprising the acts of: positioning a clock transision . . ." This is not a limiting amendment, but is made here to more clearly establish antecedent basis for subsequent limitations. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Claims 67-92 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,112,284 to Hayek et al. This rejection is respectfully traversed.

Claim 67 recites a method of calibrating a data path of a digital circuit comprising, *inter alia*, the acts of: "positioning a clock transition of a clock signal at one edge of a data eye of a bit of data received on said data path; and relocating said clock transition to approximately a center of said data eye based on said one edge."

Hayek does not disclose positioning a clock transition at one edge of a data eye and relocating the same clock transition to approximately a center of said data eye. Hayek discloses "supplying a first cycle CAS# signal responsive to a master clock," (Col. 2, lines 16-17) and including a timing delay "in order to ideally time the data strobe DSTB# signal 250 in the center of the valid data window." (Col. 4, lines 25-26). Hayek does not disclose "positioning a clock transition of a clock signal at one edge of a

data eye of a bit of data received on said data path; and relocating said clock transition to approximately a center of said data eye based on said one edge.”

For at least the above reasons, Applicant respectfully requests that the rejection of claim 67 and all dependent claims be withdrawn.

Claims 73 recites a system for calibrating a data path of a digital circuit comprising, *inter alia*, “a logic circuit for positioning a clock transition of a clock signal at one edge of a data eye of a bit of data received on said data path; said logic circuit also being configured to relocate said clock transition to approximately a center of said data eye based on said one edge.”

Hayek does not disclose a logic circuit positioning a clock transition at one edge of a data eye and relocating the same clock transition to approximately a center of said data eye.

For at least the above reasons, Applicant respectfully requests that the rejection of claim 73 and all dependent claims be withdrawn.

Claim 79 recites an integrated circuit semiconductor device comprising a system for calibrating a data path of a digital circuit, the system comprising, *inter alia*, “a logic circuit for positioning a clock transition of a clock signal at one edge of a data eye of a bit of data received on said data path; said logic circuit also being configured to relocate said clock transition to approximately a center of said data eye based on said one edge.”

Hayek does not disclose a logic circuit positioning a clock transition at one edge of a data eye and relocating the same clock transition to approximately a center of said data eye.

For at least the above reasons, Applicant respectfully requests that the rejection of claim 79 and all dependent claims be withdrawn.

Claim 86 recites a processor system, comprising, inter alia, "a processor; and a dynamic random access memory (DRAM) coupled to said processor, at least one of said processor and memory having a system for calibrating a data path of a digital circuit, said system for calibrating comprising: a logic circuit for positioning a clock transition of a clock signal at one edge of a data eye of a bit of data received on said data path; said logic circuit also being configured to relocate said clock transition to approximately a center of said data eye based on said one edge."

Hayek does not disclose a logic circuit positioning a clock transition at one edge of a data eye and relocating the same clock transition to approximately a center of said data eye.

For at least the above reasons, Applicant respectfully requests that the rejection of claim 86 and all dependent claims be withdrawn.

Claims 67-92 stand rejected under the doctrine of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 6, 11, 16, 26, 33, 34, 42, 49, 52, 59 and 60 of U.S. Patent No. 6,691,214 to Li et al. This rejection is respectfully traversed.

Claim 1 of Li recites "[a] method of calibrating a data path of a digital circuit, said method comprising: clocking an input data signal on said data path into said digital circuit using a clock signal, each bit of said input data signal having a data eye during which said bit is valid; adjusting the relative timing of said input data signal with respect to said clock signal to position a clocking transition of said clock signal at

an edge of said data eye; and further adjusting the relative timing of said input data signal with respect to said clock signal by moving the data signal relative to the clock signal by a predetermined amount which is approximately equal to one-half of a width of said data eye to position said clocking transition at approximately a center of said data eye.”

The Office Action does not point to any evidence showing how present claims 67-92 are obvious from claim 1 of Li. The scope of claims 67-92 differ from claim 1 of Li in many important respects: for example, claim 67 claims the step of “positioning a clock transition of a clock signal at one edge of a data eye.” None of claim 1 of Li or any other claim of Li discloses this limitation; the Office Action merely states that the present claims are a subset of claim 1, but this cannot be correct because all of the claims of Li lack this and other limitations. The Office Action does not point to any other points of obviousness. An analysis of claims 6, 11, 16, 26, 33, 34, 42, 49, 52, 59 and 60 of Li yields the same result.

Application No. 10/751,437
Amendment dated March 28, 2006
Reply to Office Action of December 28, 2006

Docket No.: M4065.0271/P271-A

For at least the above reasons, Applicant respectfully requests that the rejection of claims 67-92 be withdrawn. In view of the above amendment, Applicant believes the pending application is in condition for allowance.

Dated: March 28, 2006

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

Jerome A. DeLuca

Registration No.: 55,106

DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorneys for Applicant